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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,866	08/04/2003	Takeshi Yoshida	241190US2	4630

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,866	YOSHIDA, TAKESHI	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9* is/are rejected.

7)☒ Claim(s) *7,8,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/4/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-6, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Adusumilli (US 6,418,545 B1).

Regarding claim 1, Adusumilli discloses a semiconductor integrated circuit comprising:

a system bus (path from 213 to 214 in Fig. 3) divided into stages and configured to transfer signals;

stage elements (223, 341-343, 224) configured to connect the stages in series and operate in a divided mode (normal mode) transferring signals (normal input 213) from a stage on an input side (223) to a stage on an output side (224) in synchronization with a clock signal (clock 450 in Fig. 4) and in a through mode (BSC mode) that always passes signals (TDI signal) from the stage on the input side (223) to the stage on the output side (224); and

a plurality of function modules (331, 332) connected to the different stages.

Regarding claim 2, Adusumilli discloses a clock transfer circuit (one that generates clock 450) configured to supply the clock signal to the stage elements in the divided mode and stop the supply of the clock signal to the stage elements in the through mode (by switching 711 in Fig. 7 to JTAG_TCK 787; therefore, supply of CLK 718 will stop).

Regarding claim 3, Adusumilli discloses that the function modules have equivalent functions (see 331, 332).

Regarding claim 5, Adusumilli discloses that each of the stage elements comprises a storage circuit (see 493, 495 in Fig. 4) configured to hold a signal transferred from the stage on the input side.

Regarding claim 6, Adusumilli discloses that the storage circuit is a flip-flop circuit (SCAN DFF 493, 495 in Fig. 4) configured to latch and hold the signal in synchronization with the clock signal (clock 450).

Regarding claim 9, Adusumilli discloses that the stage element comprises a clock controller (711) configured to supply clock signals (CLK 718) to the flip-flop circuit in the divided mode, and in the through mode, stop the supply of the clock signals (by switching 711 in Fig. 7 to JTAG_TCK 787; therefore, supply of CLK 718 will stop) to the flip-flop circuit and keep the storage circuit passing the signal therethrough.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adusumilli.

As applied previously, Adusumilli teaches all the features of the claimed invention, with the exception of teaching the claimed function modules that are each a memory having a function of storing data.

However, Adusumilli teaches functional logic that can be any logic circuit such as memory.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the functional logic of Adusumilli with the memory in order to store incoming data.

Allowable Subject Matter

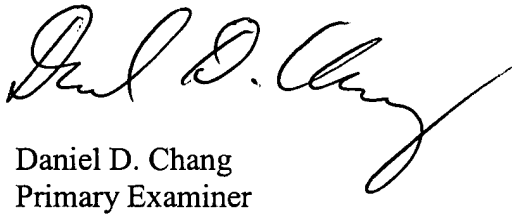
Claims 7, 8, 10, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER